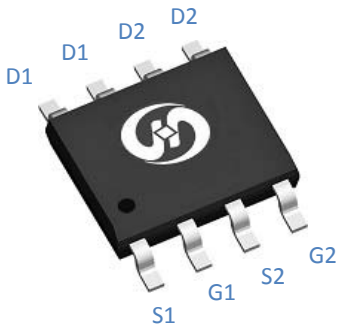
40V Dual N+P Channel Power MOSFET

	N-CH	P-CH	
V_{DS}	40	-40	V
$R_{DS(on),max}$	22	42	mΩ
$I_{D\ (Sillicon\ Limited)}$	7.5	-6	A

Feature

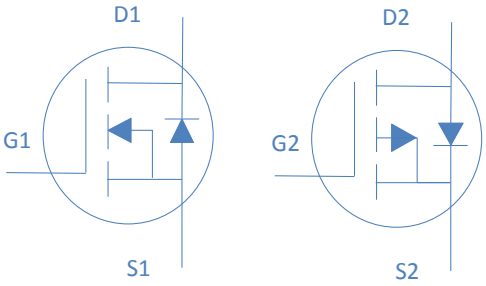
◇ High Speed Power Switching, Logic Level
◇ Enhanced Avalanche Ruggedness
◇ Lead Free, Halogen Free

SOIC-8



Application

◇ Hard Switching and High Speed Circuit
◇ BLDC motor



Part Number	Package	Marking
HTS220C04	SO8	TS220C04

Absolute Maximum Ratings at T_j=25℃ (unless otherwise specified)

Parameter	Symbol	Conditions	N-CH	P-CH	Unit
Continuous Drain Current (Silicon Limited)	I_D	T_A=25℃	7.5	-6	A
		T_A=100℃	6	-5	
Drain to Source Voltage	V_{DS}	-	40	-40	V
Gate to Source Voltage	V_{GS}	-	±20		V
Pulsed Drain Current	I_{DM}	-	30	-24	A
Power Dissipation	P_D	T_A=25℃	2		W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to150		℃

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	62.5	℃/W
Thermal Resistance Junction-Case	$R_{\theta JC}$	25	℃/W

N-Channel Electrical Characteristics at T_j=25℃ (unless otherwise specified)

Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250μA	40	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250μA	1.5	2.0	3.0	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V, V_{DS}=32V, T_j=25℃	-	-	1	μA
		V_{GS}=0V, V_{DS}=30V, T_j=125℃	-	-	25	
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=7.5A	-	20	22	mΩ
		V_{GS}=4.5V, I_D=5A	-	33	40	
Transconductance	g_{fs}	V_{DS}=5V, I_D=7.5A	-	20	-	S

Dynamic Characteristics

Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=20V, f=1MHz	-	536	-	pF
Output Capacitance	C_{oss}		-	83	-	
Reverse Transfer Capacitance	C_{rss}		-	66	-	
Total Gate Charge	Q_g(10V)	V_{DD}=20V, I_D=7.5A, V_{GS}=10V	-	14.5	-	nC
Gate to Source Charge	Q_{gs}		-	2.1	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	4.3	-	
Turn on Delay Time	$t_{d(on)}$	V_{DD}=10V, I_D=1A, V_{GS}=10V, R_G=6Ω,	-	5	-	ns
Rise time	t_r		-	10	-	
Turn off Delay Time	$t_{d(off)}$		-	15	-	
Fall Time	t_f		-	12	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_F=7.5A	-		1.3	V

Fig 1. Typical Output Characteristics

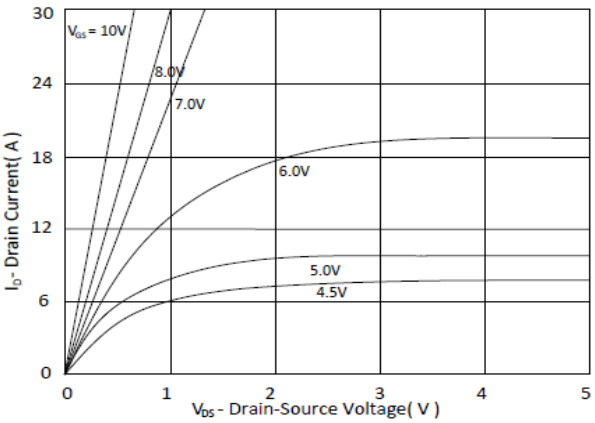


Figure 2. On-Resistance vs. Gate-Source Voltage

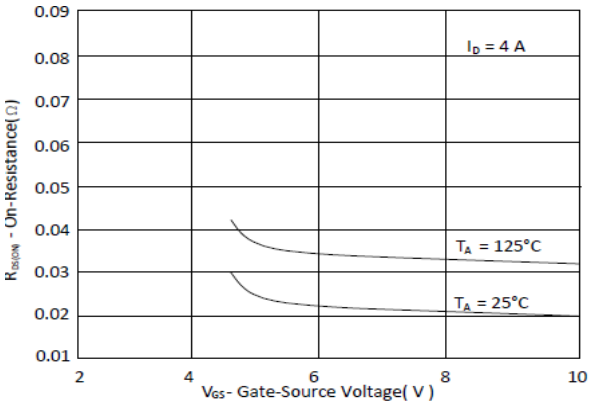


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

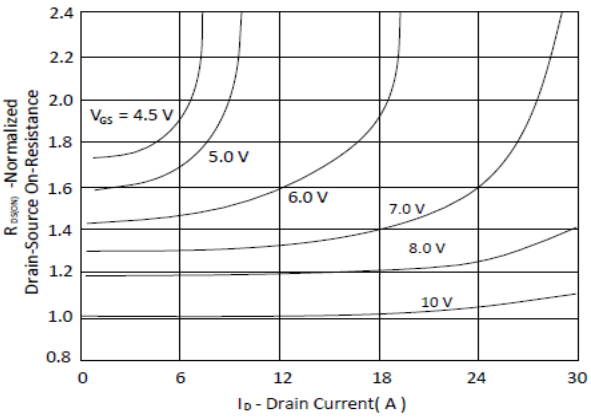


Figure 4. Normalized On-Resistance vs. Junction Temperature

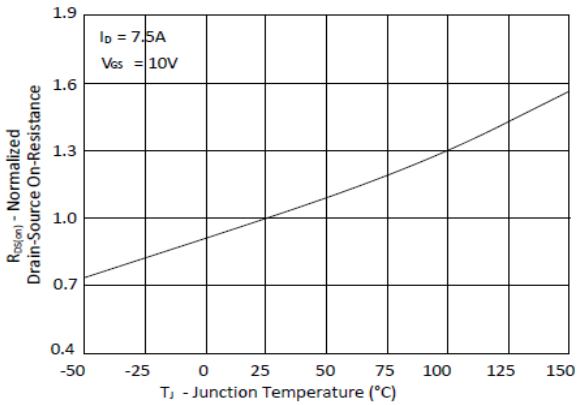


Figure 5. Typical Transfer Characteristics

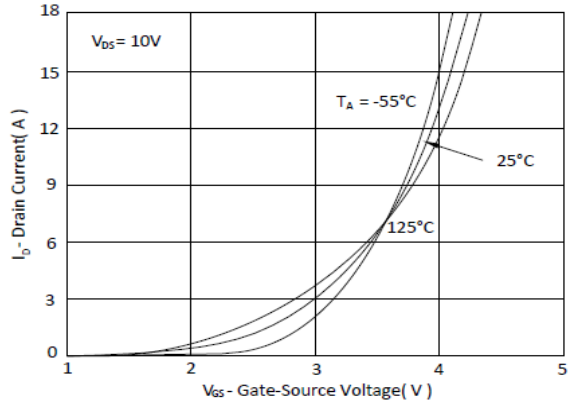


Figure 6. Typical Source-Drain Diode Forward Voltage

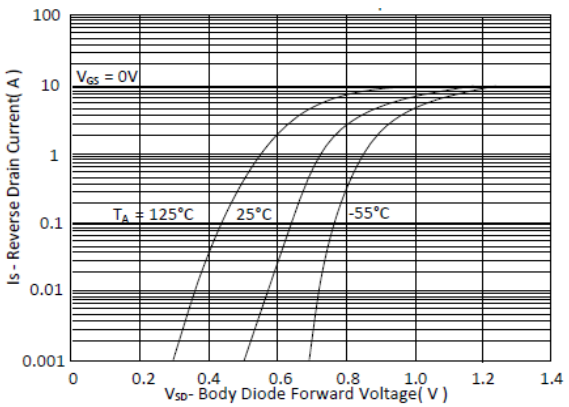


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

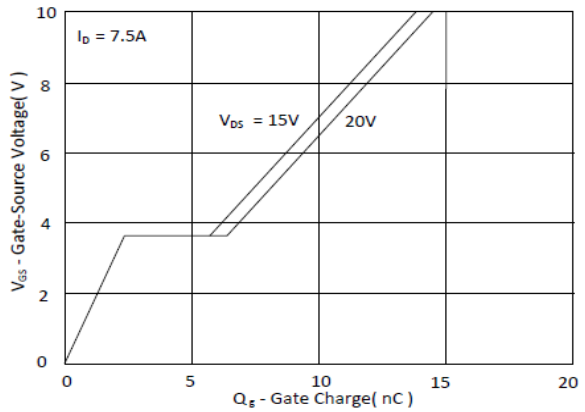


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

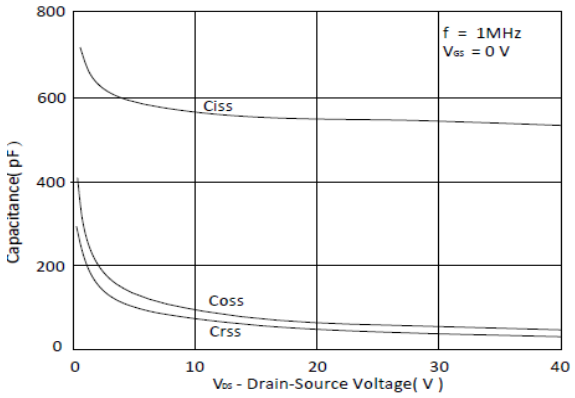


Figure 9. Maximum Safe Operating Area

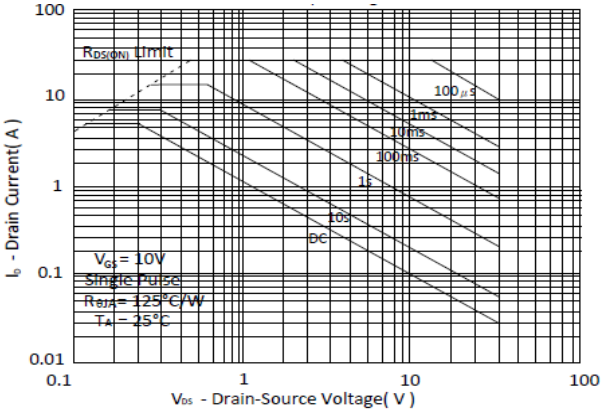


Figure 10. Single Pulse Maximum Power Dissipation

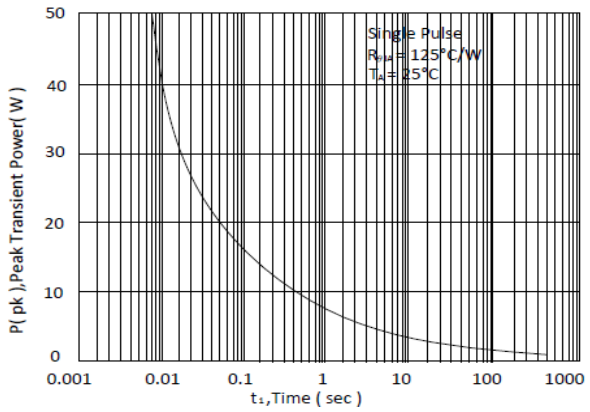
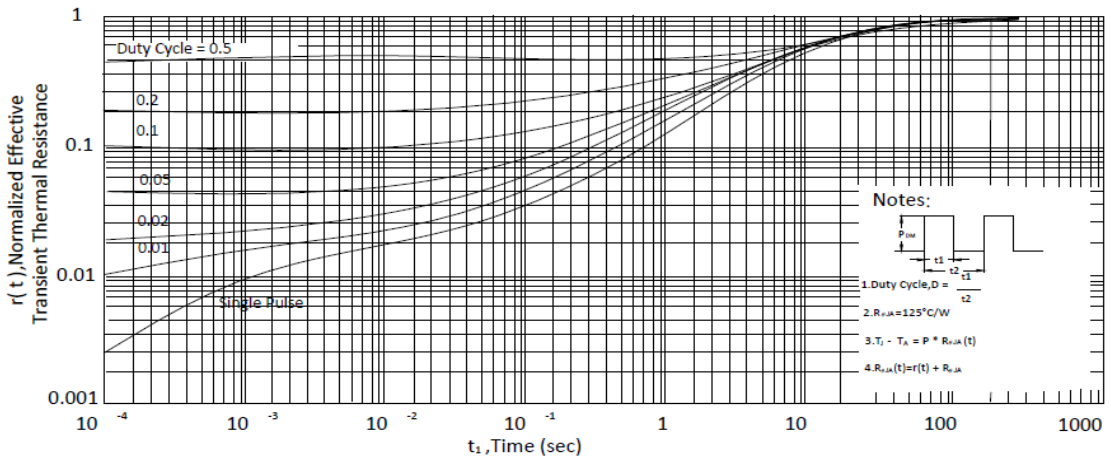
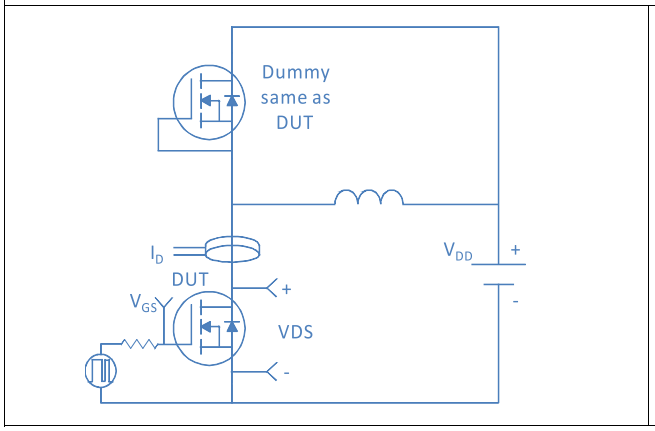
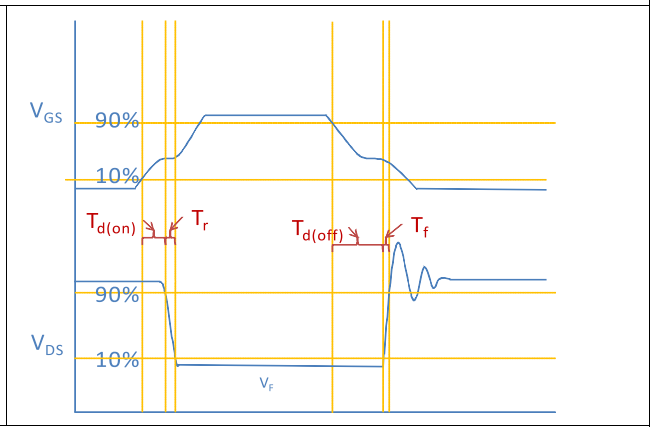


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient

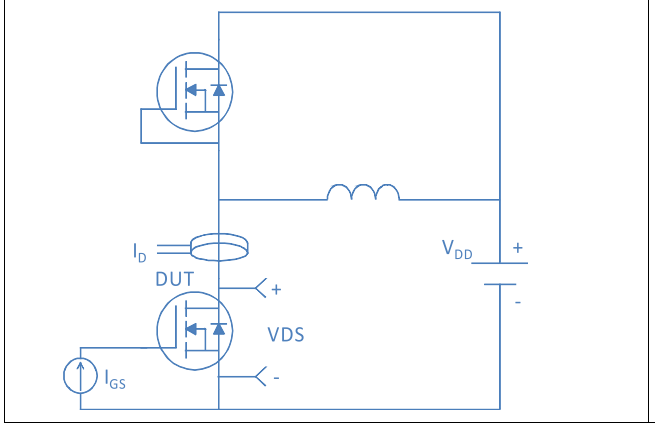


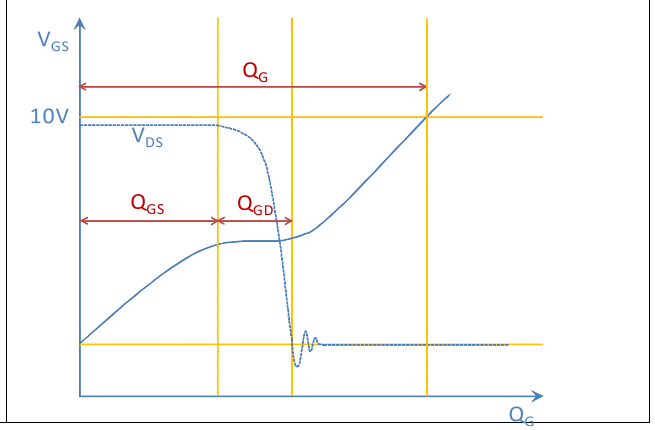
Inductive switching Test



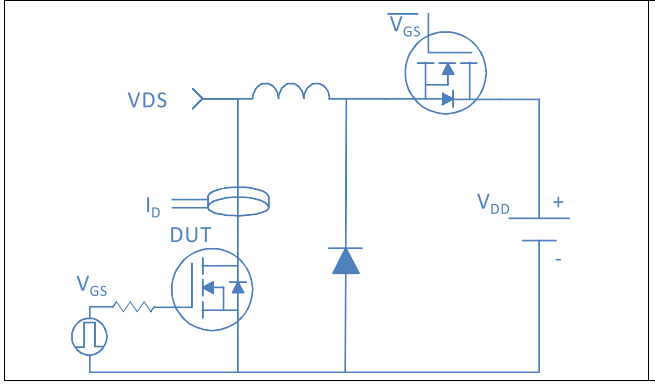


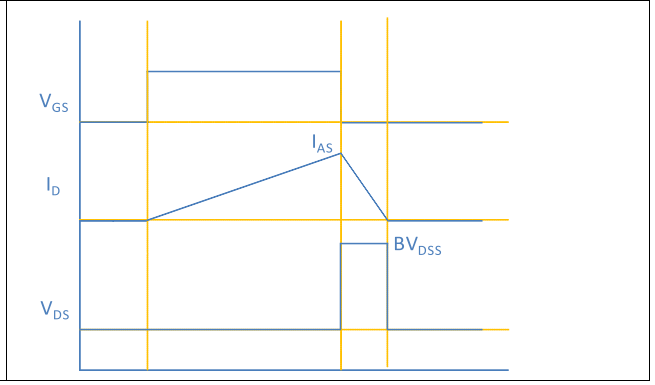
Gate Charge Test



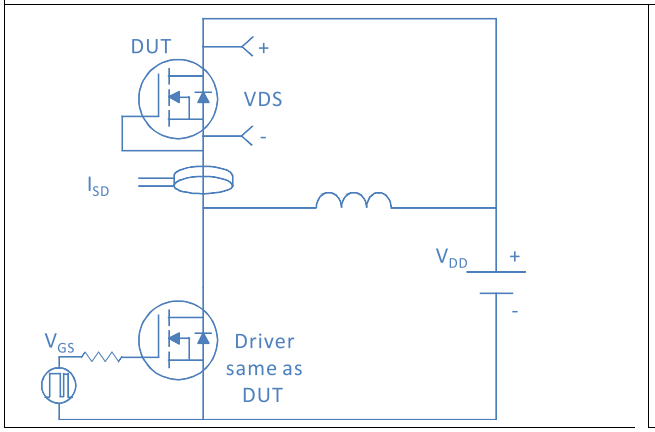


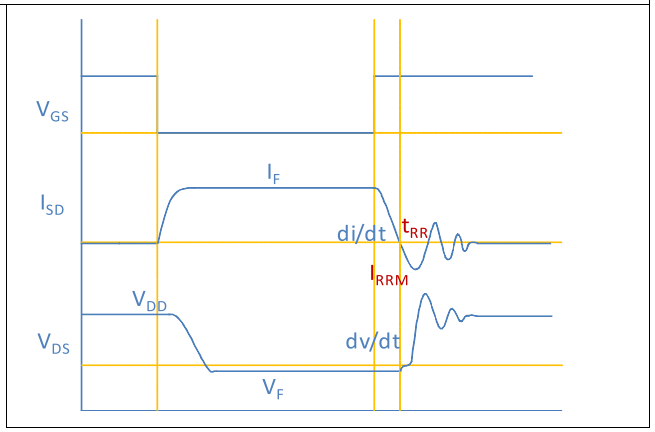
Uclamped Inductive Switching (UIS) Test





Diode Recovery Test





P-Channel Electrical Characteristics at T_j=25℃ (unless otherwise specified)

Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=-250μA	-40	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=-250μA	-1.5	-2.0	-3.0	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V, V_{DS}=-32V, T_j=25℃	-	-	-1	μA
		V_{GS}=0V, V_{DS}=-30V, T_j=125℃	-	-	-25	
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=-10V, I_D=-6A	-	37	42	mΩ
		V_{GS}=-4.5V, I_D=-4A	-	70	85	
Transconductance	g_{fs}	V_{DS}=-5V, I_D=-6A	-	10	-	S

Dynamic Characteristics

Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=-20V, f=1MHz	-	810	-	pF
Output Capacitance	C_{oss}		-	94	-	
Reverse Transfer Capacitance	C_{rss}		-	72	-	
Total Gate Charge	Q_g (10V)	V_{DD}=-20V, I_D=-6A, V_{GS}=-10V	-	15.0	-	nC
Gate to Source Charge	Q_{gs}		-	2.6	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	3.1	-	
Turn on Delay Time	$t_{d(on)}$	V_{DD}=-10V, I_D=-1A, V_{GS}=-10V, R_G=6Ω,	-	12	-	ns
Rise time	t_r		-	15	-	
Turn off Delay Time	$t_{d(off)}$		-	25	-	
Fall Time	t_f		-	15	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_F=-6A	-		-1.3	V

Fig 1. Typical Output Characteristics

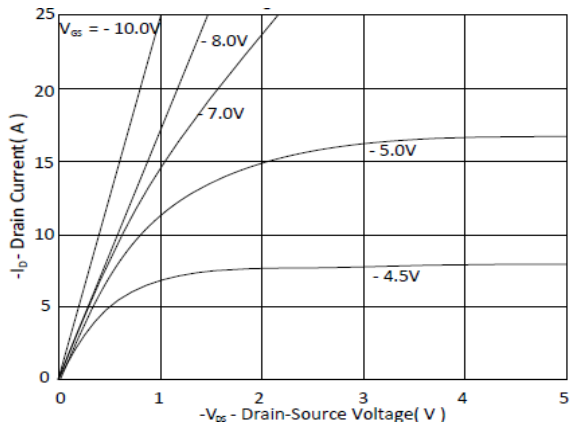


Figure 2. On-Resistance vs. Gate-Source Voltage

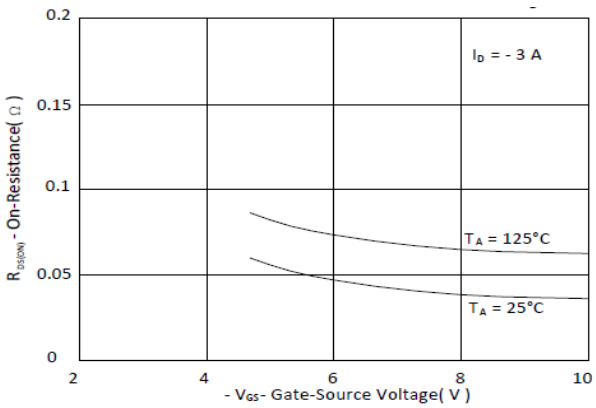


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

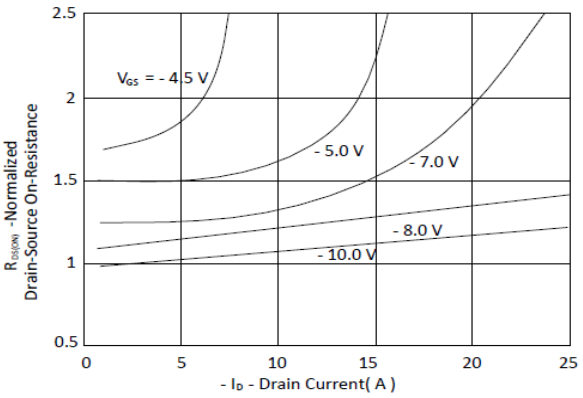


Figure 4. Normalized On-Resistance vs. Junction Temperature

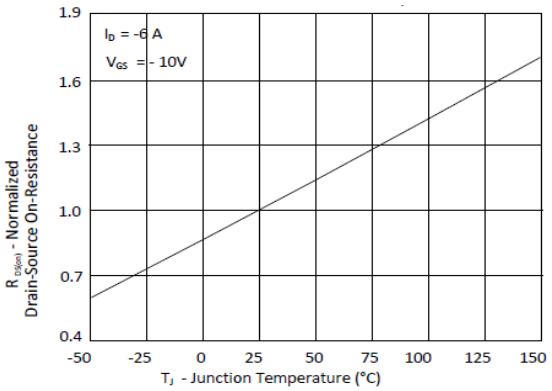


Figure 5. Typical Transfer Characteristics

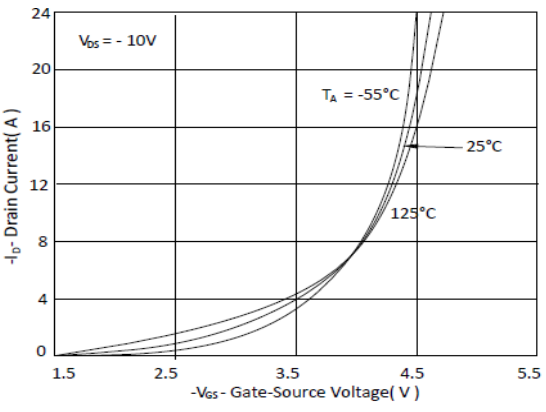


Figure 6. Typical Source-Drain Diode Forward Voltage

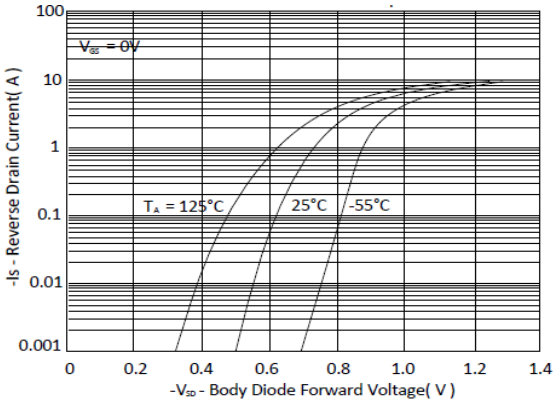


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

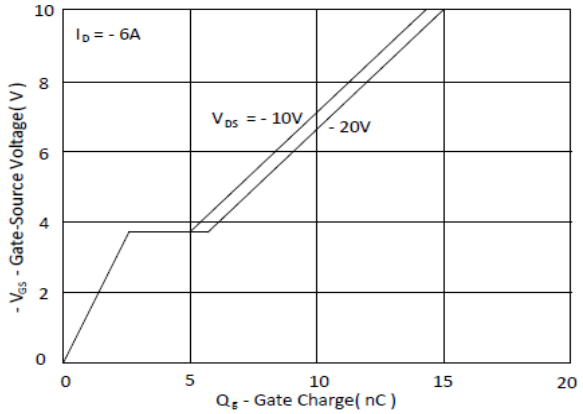


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

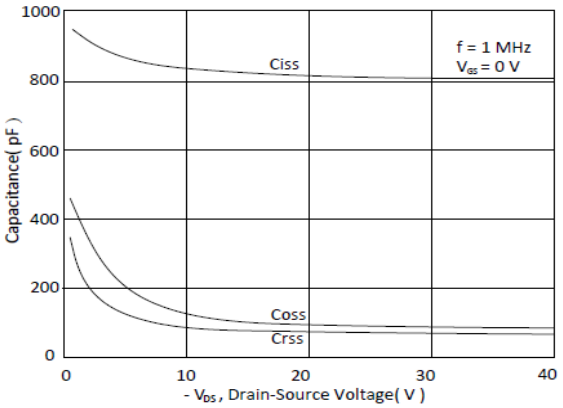


Figure 9. Maximum Safe Operating Area

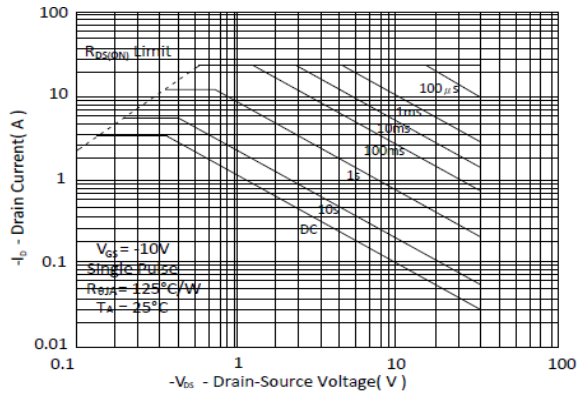


Figure 10. Single Pulse Maximum Power Dissipation

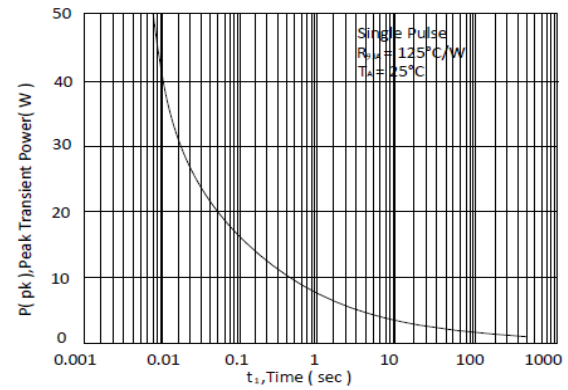
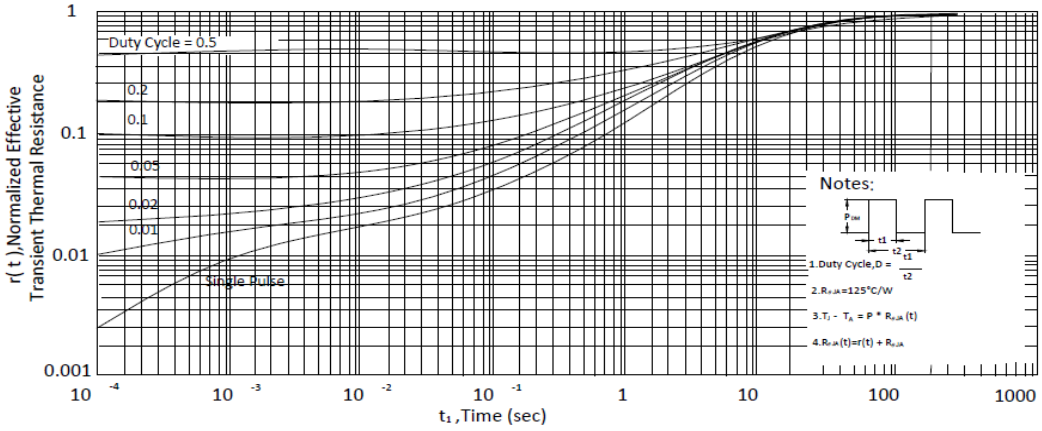
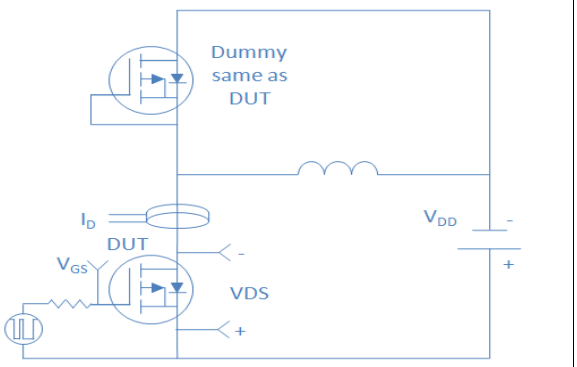
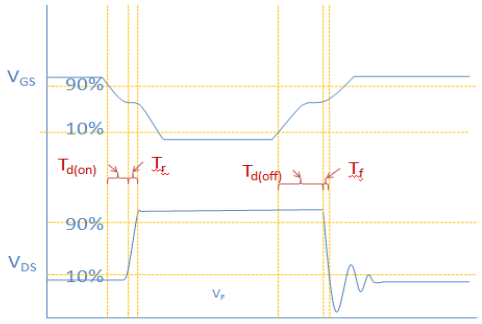


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient

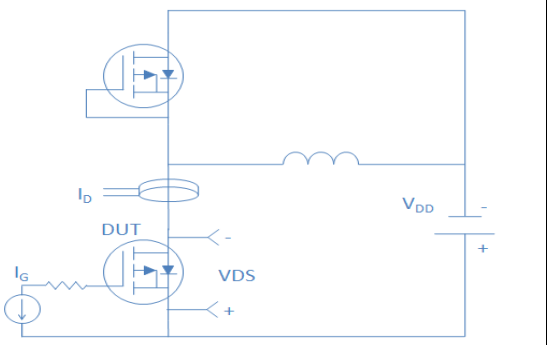


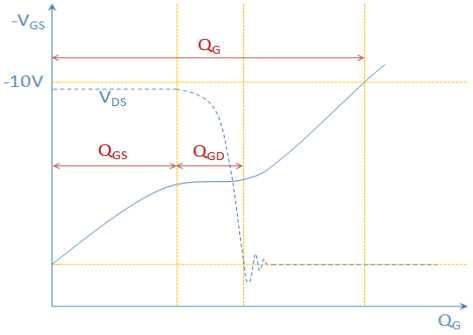
Inductive switching Test



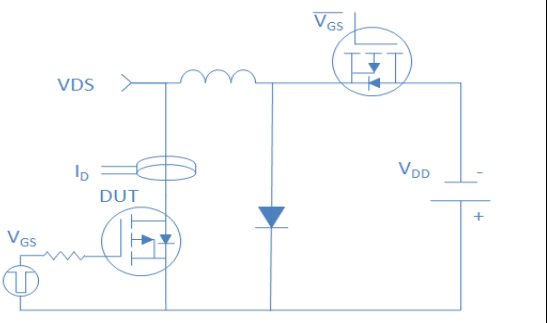


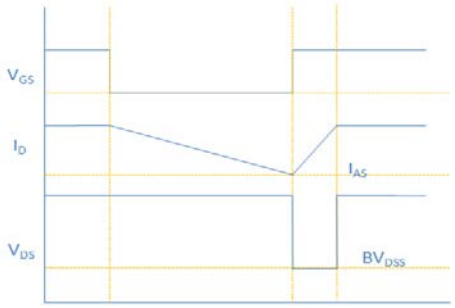
Gate Charge Test



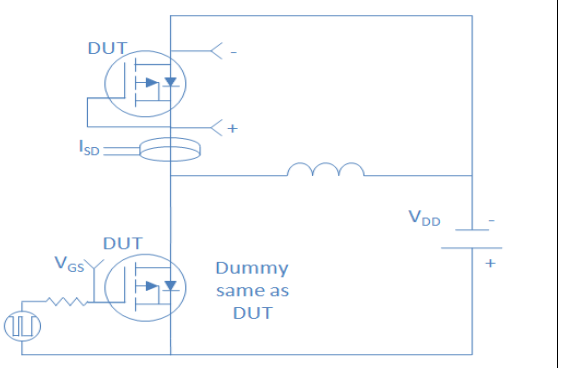


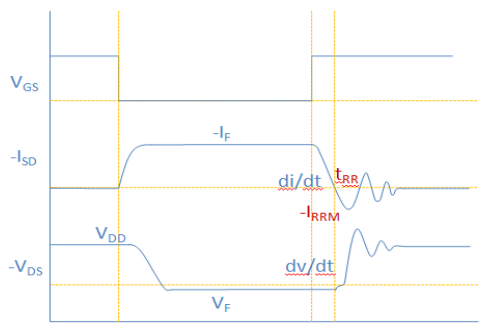
Uclamped Inductive Switching (UIS) Test





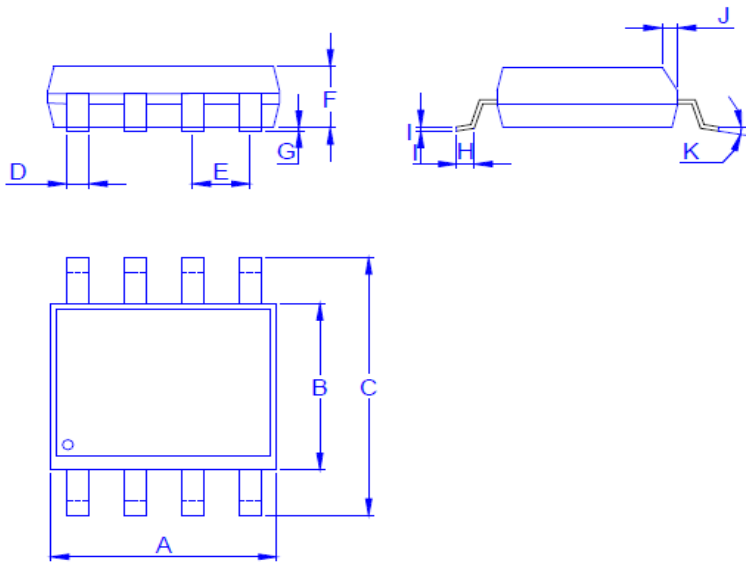
Diode Recovery Test





Package Outline

SOIC-8, 8leads



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K
Min.	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25	0°
Typ.					1.27						
Max.	5.10	4.10	6.20	0.51		1.62	0.28	0.83	0.26	0.50	8°